

Verification (UVM) Services

At Fidus Systems, we understand the unique challenges faced by technology companies – too many projects and too few engineering resources. With top engineering talent, multiple design centers and on-site staffing options, Fidus provides highly responsive engineering teams that are an extension of your development team to successfully bring products to market faster.

Recognized as a trusted design partner, Fidus is dedicated to meeting customer expectations, and developing long-term relationships with clients built on integrity, quality and open communications.

Fidus is pleased to provide customers with full end-to-end development solutions or more selective targeted engagements.

Fidus has delivered more than 4000+ projects for 400+ customers, from Tier-1 multinationals to SMEs to start-ups. Fidus is headquartered in Ottawa, Canada with local design centers in Kitchener-Waterloo and Silicon Valley.

HOW WE HELP

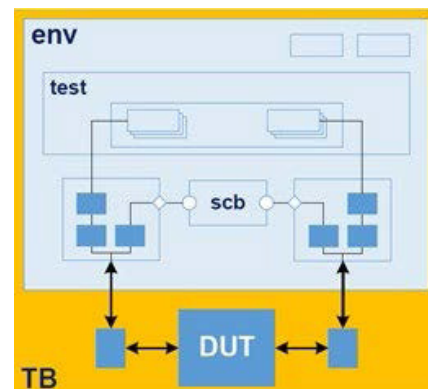
Fidus has extensive experience in Digital Design Verification through the planning and implementation of re-usable verification environments, and supports UVM™, SystemVerilog, and SystemC® software.

We preserve your investment in legacy simulation environments/tools, help you transition to newer methodologies, and build new verification environments to achieve your quality goals.

VERIFICATION EXPERTISE

- **Directed Testing:** For simple FPGA flows, we can offer Directed Testing.
- **Expertise:** We do full FPGA and ASIC/SoC verification, using UVM, SystemVerilog, and SystemC.
- **Engagement Models:** We offer flexible engagement models, ranging from consulting to full turnkey verification environments.
- **Test Bench Migration:** We can migrate your directed test benches to methodology based, reusable, coverage driven, constrained random testbench environments with live tracking capabilities.
- **Team Bring Up:** We offer planning and configuration set-up that will train your development and management teams on the benefits, savings, and de-risking techniques leveraged in Verification.

- **Verification Planning:** In scenarios where we bring specific domain expertise, we can provide the entire planning process. When the domain expertise resides with you, we provide consulting to coordinate your planning effort. In addition, we help you reach your quality goals through feature categorizing and live test-plan creation.
- **Verification IP:** We source verification IPs for standard protocols like AMBA, AXI, PCIe, SRIO PCIe Bridging, NVMe, WiFi 802.11 variant PHY and MACs, Ethernet, DDR, USB, SATA, AHCI, SerDes, UART, I2C, DDR, HDLC controllers, etc.
- **Constrained Random Verification (CRV):** We offer constrained random verification services to augment your existing environments.
- **Assertion-Based Verification (ABV):** We can train your design and verification teams on Assertion-Based Verification and will bind, track and measure these in your existing environments.



FIDUS - PREMIER AMD ADAPTIVE COMPUTING PARTNER

AMD enables smarter, connected, and differentiated systems, integrating the highest levels of software- based intelligence with hardware optimization and any-to-any connectivity. By invitation, Fidus became the Inaugural Premier Design Services Partner for AMD Adaptive Computing (formerly Xilinx). As a Premier Design Partner, Fidus receives exclusive training, certification, and early access to tools, IP and new silicon. With ever-increasing requirements for designers to conduct thermal simulations, Fidus provides you with access to thermal simulation tools and the required resources to run your specific thermal simulations. Ease your cost and support burden and leverage the expertise, experience and tools from Fidus.



EXAMPLES OF OUR WORK

FPGA Verification

- Numerous FPGA vendors/families (e.g.Xilinx®, Intel®/Altera™)
- Diverse set of systems and protocols, including DSP
- Full range from Directed Testing for simpler FPGAs to Constrained Random/UVM Verification for complex FPGAs

ASIC Verification

- Wireless signal processors/60G Wireless Modems
- High Performance Virtualized Network Interface
- Controllers
- High-end Server Processors
- DDR Clock Driversand Buffers
- PCIe Bridges
- Mixed analog and digital designs

TASKS UNDERTAKEN

- Translate design specs into verification requirements
- Architect block/top level verification environments
- Develop verification plans, schedule estimation, and tracking
- Enhance pre-existing verification environments with UVM verification methodologies
- Design and implement verification components; reference models, scoreboards, agents, etc.
- Integrate bit accurate reference models from MATLAB into functional SystemVerilog test-benches (e.g. DSP)
- Incorporate and configure external Verification IP
- Implement coverage models, collect coverage data, and achieve coverage closure
- Manage simulation regressions, triage and fix regression failures
- Adopt and support continuous integration techniques related to hardware development
- Investigate, evaluate, and recommend new tools in the spirit of continuous improvement
- Create scripts for improved verification productivity
- Collaborate with rapid prototyping, test, validation, and software teams

20+
years experience

Collaborating with smart teams is what fuels us every day.

4,000+
successful projects

Your unique challenges are our obsession.

400+
customers

Extending your team with our expertise brings designs to market faster.

95%
repeat customers

Customers love to work with us, again and again.

ABOUT FIDUS

For over 25 years, Fidus has been delivering electronic product design and embedded system solutions for extraordinarily complex, high bandwidth and low latency projects. Our FPGA and ASIC, hardware, software, verification, mechanical, and signal integrity teams work to innovate, design and deliver next-generation products for customers in emerging technology markets. With over 400 customers and 4000+ completed projects, we have teams of domain experts available to extend your capacities seamlessly and commitment to getting designs and prototypes to market faster, and right the first time.